DOCKET NO.: WEST14-00018 **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paul F. Struhsaker, et al
Serial No.:	09/839,509
Filed:	April 20, 2001
For:	BACKPLANE ARCHITECTURE FOR USE IN WIRELESS AND WIRELINE ACCESS SYSTEMS
Group No.:	2616
Examiner:	Ian N. Moore

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief dated November 8, 2006, the Applicant is submitting a Substitute Appeal Brief.

A one-month extension of time is believed to be necessary. An appropriate petition and fee are enclosed.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: 1-8-2007

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DOCKET NO.: WEST14-00018 **PATENT**
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Paul F. Struhsaker, et al.
Serial No.	:	09/839,509
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For	:	BACKPLANE ARCHITECTURE FOR USE IN WIRELESS AND WIRELINE ACCESS SYSTEMS
Group No.	:	2661
Examiner	:	Ian N. Moore

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Sir:

SUBSTITUTE APPEAL BRIEF

This Brief is submitted on behalf of Appellant for the application identified above. A one-month extension of time is believed to be necessary. An appropriate petition and fee are enclosed. Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, ACCESS SOLUTIONS, LTD.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–20 are pending in the present application. Claims 10–13 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,091,729 to *Dove*. Claims 1–4 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,760,327 to *Manchester et al* in view of U.S. Patent No. 6,560,219 to *Tabu et al*. Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of U.S. Patent No. 6,512,769 to *Chui et al*. Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of U.S. Patent No. 6,047,348 to *Lentz et al*. Claims 7–8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al*. Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of U.S. Patent No. 5,355,090 to *Pajowski et al*. Claims 14–16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dove*. Claims 18–19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of U.S. Patent No. 5,416,776 to *Panzarella et al*. The rejections of pending claims 1–20 is appealed.

STATUS OF AMENDMENTS

No amendment to the claims was filed following the final Office Action mailed May 3, 2005.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages but does not delimit any of the claimed inventions.

In General:

The present invention relates to a backplane architecture for wireless/wireline equipment. The diversity of different broadband access technologies available (wireline access through cable modems, digital subscriber lines, and/or fiber optic connections, and various wireless standards such as IEEE 802.16) has resulted in non-standardized, widely varying backplane architectures in access equipment. Specification, page 11, line 14 through page 12, line 20; U.S. Patent Application Publication No. 2004/0213188, ¶¶ [0055] –[0056]. As a result, maintenance and other services (e.g., upgrades) is more costly due to the lack of backplane architecture standardization. Specification, page 12, lines 10–20; U.S. Patent Application Publication No. 2004/0213188, ¶ [0056].

The claimed invention proposes a backplane architecture suitable for different types of wireless/wireline broadband access equipment, including access processors, remote modems, and combined access processors and remote modems. Specification, page 14, lines 2–20; U.S. Patent Application Publication No. 2004/0213188, ¶¶ [0058]–[0061]. The backplane architecture 210 of the present invention includes: a low tier (parallel) bus 410 supporting cell-based traffic, such as Asynchronous Transfer Mode (ATM) switched traffic, and supporting data rates of up to

approximately 2 gigabits per second; and a high tier bus 415 providing high speed serial links supporting data rates of up to 20 gigabits per second:

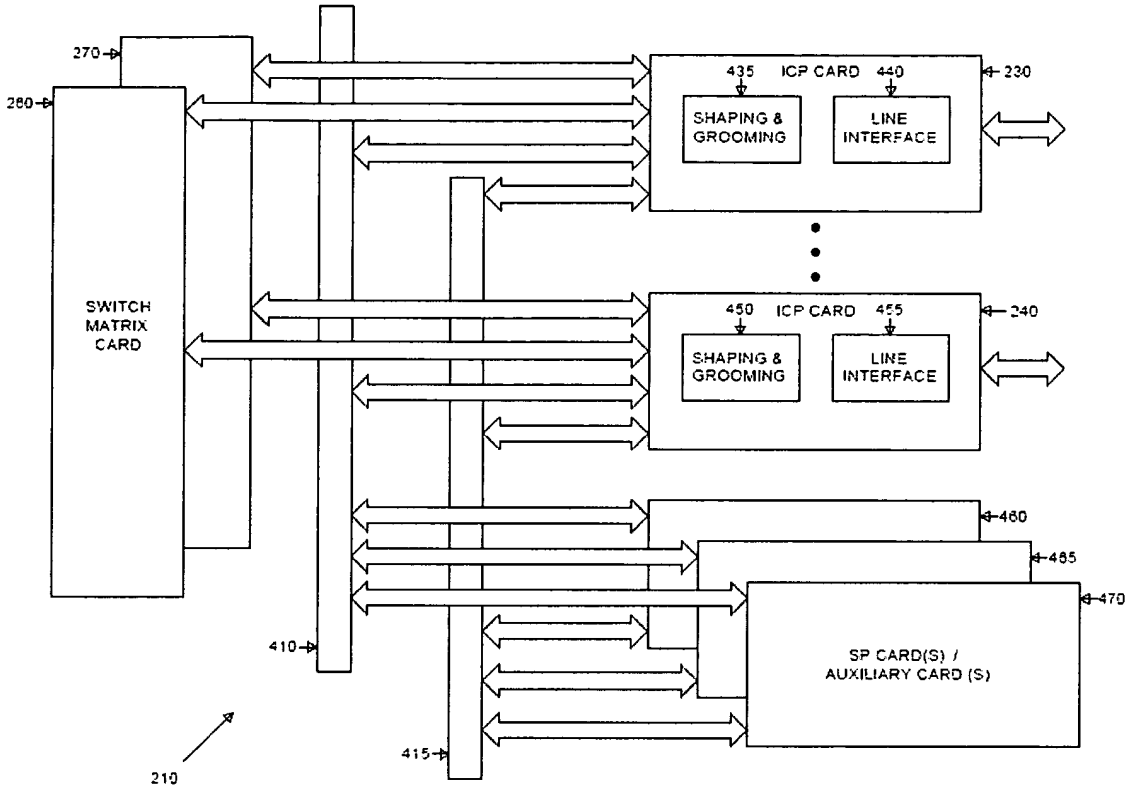

FIGURE 4

Specification, Figure 4, page 31, line 4 through page 32, line 4, page 32, line 20 through page 33, line 11; U.S. Patent Application Publication No. 2004/0213188, Figure 4, ¶¶ [0101]–[0102], [0105]–[0106]. The low tier bus 410 provides a switch fabric across the backplane allowing switching between circuit boards on the input side and circuit boards on the output side.

Specification, page 31, line 20 through page 32, line 4; U.S. Patent Application Publication No. 2004/0213188, ¶ [0102].

Backplane 210 may be employed for an access processor shelf 170, for a remote modem shelf 140, or both. Specification, page 25, lines 11–20 and page 27, line 16 through page 28, line 4; U.S. Patent Application Publication No. 2004/0213188, ¶¶ [0085], [0092]. In either use, multiple interface control processor 230 and 240, 330 and 340 are supported. Specification, Figure 2, page 26, lines 6–20 and Figure 3, page 28, line 23 through page 29, line 15; U.S. Patent Application Publication No. 2004/0213188, Figure 2 and 3, ¶¶ [0087], [0095]. Multiple serial links are provided for each interface control processor slot within the backplane. Specification, page 33, line 23 through page 34, line 4; U.S. Patent Application Publication No. 2004/0213188, ¶ [0108].

In various embodiments, the low tier bus uses 32 bit data paths, wraps ATM cells with a header to allow switching based on a software connection map, and provides redundant clock references. Specification, page 31, line 15 through page 32, line 19; U.S. Patent Application Publication No. 2004/0213188, ¶¶ [0102]–[0104].

Support for Independent Claims:

Per 37 C.F.R. § 41.37, only support for the independent claims is discussed herein. The discussion of the claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.

In the embodiment to which independent claim 1 is directed, a backplane for use with processors and modems in wireless and wireline access includes a low tier cell-based bus 410 capable of aggregate traffic rates of up to approximately two gigabits per second and one or more high tier serial links 415 capable of aggregate traffic rates of up to approximately twenty gigabits per second. Specification, Figure 4, page 31, line 4 through page 32, line 4, page 32, line 20 through page 33, line 11.

In the embodiment to which independent claim 10 is directed, a backplane for use with processors and modems in wireless and wireline access includes a high tier bus 415 comprising one or more high speed serial links capable of aggregate traffic rates of up to approximately twenty gigabits per second. Specification, Figure 4, page 31, line 4 through page 32, line 4, page 32, line 20 through page 33, line 11.

In the embodiment to which independent claim 20 is directed, a wireless/wireline access device includes a backplane having a low tier cell-based bus 410 capable of aggregate traffic rates of up to approximately two gigabits per second and one or more high tier serial links 415 capable of aggregate traffic rates of up to approximately twenty gigabits per second. Specification, Figure 4, page 31, line 4 through page 32, line 4, page 32, line 20 through page 33, line 11. The device also includes an access processor unit, a modem unit, and a combined access processor and modem unit. Specification, Figure 2, page 26, lines 6–20 and Figure 3, page 28, line 23 through page 29, line 15.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 10–13 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Dove*. Claims 1–4 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al*. Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Chui et al*. Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Lentz et al*. Claims 7–8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al*. Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Pajowski et al*. Claims 14–16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dove*. Claims 18–19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Panzarella et al*.

ARGUMENT

1. The rejection of claims 10–13 and 17 under 35 U.S.C. § 102(e) as being anticipated by *Dove*.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-73 (8th ed. rev. 2 May 2004).

a. The recited serial link(s) are not found in the cited reference.

Independent claim 10 recites that the high tier bus comprises one or more serial links. Such a feature is not found in the cited reference. The cell bus 550 disclosed in *Dove* that is cited in the final rejection as satisfying the serial link limitation includes eight parallel bits or signal lines, and is therefore a parallel bus. *Dove*, column 4, lines 24–27, column 7, lines 47–48.

The final rejection states:

> . . . see FIG. 5, each cell bus/link 550 transmits cells serially, thus, each link/bus 550 is a serial link . . .

Paper No. 20050429, page 3. However, such an interpretation of "serial link" (that is, that some quantum of data, no matter how large, is transmitted serially over the link) is contrary to the ordinary and accepted meaning of the term.

As an initial matter, it should be noted that the cited reference provides no support for the interpretation proffered in the Office Action. *Dove* does not use the term "serial" anywhere therein, and particularly not in connection with cell bus 550.

The interpretation is also inconsistent with the specification of the subject application, which differentiates low tier cell bus 410, a cell-based bus of the type disclosed in *Dove*, from high tier serial links 415, the serial links recited in the claim. Compare Specification, page 31, line 4 through page 32, line 4 (U.S. Patent Application Publication No. 2004/0213188, ¶ [0101]–[0102]) with Specification, page 32, line 20 through page 33, line 11 (U.S. Patent Application Publication No. 2004/0213188,¶ [0105]–[0106]). Because the specification as filed compels an interpretation of "serial link" as excluding cell-based buses such as cell bus 450 in *Dove*, the interpretation asserted in the final rejection – even if reasonable (which Appellants dispute) – cannot be accepted. *In re Johnston*, 435 F.3d 1381, 1384 (Fed. Cir. 2006) (broader interpretations of claim limitations "must give way to the meaning imparted by the specification"), citing *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

The interpretation is also inconsistent with the ordinary usage of the term. U.S. Patent No. 6,760,327 to *Manchester et al*, for example, specifies that serial link 76 includes a single data signal. *Manchester et al*, column 8, lines 52–53.

The cell bus 450 in *Dove* transmits entire cells (53 bytes) of data concurrently, NOT bitwise, and therefore does NOT comprise a "serial link."

b. The recited at least two serial link are not found in the cited reference.

Dependent claim 17 recites that the backplane comprises at least two high speed serial links for each interface control processor slot in the backplane. Such a feature is not found in the cited

reference. The final rejection cites (Paper No. 20050429, page 3) the existence of cell clock 530 and cell sync 540 within Figure 5 of *Dove* as satisfying this limitation:

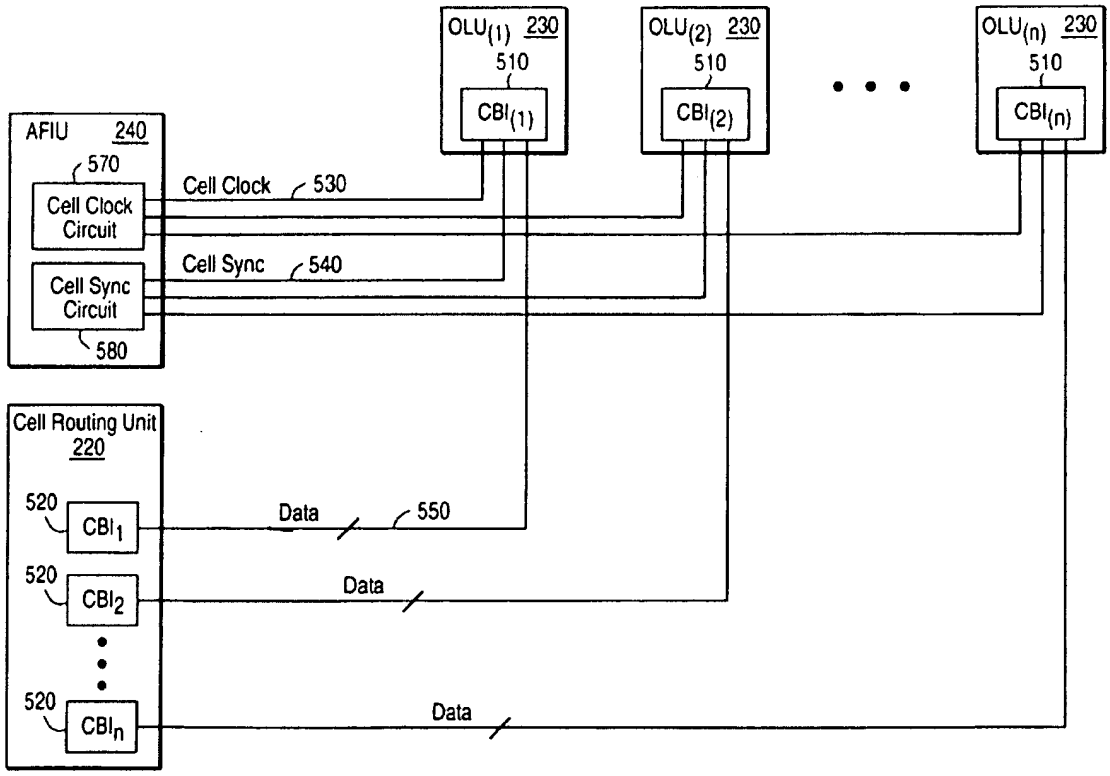

FIG_5

Dove, Figure 5. Figure 5 of *Dove* depicts only a single ATM fiber bank interface unit (AFIU) 240 (an interface control processor) and a plurality of optical line units (OLUs) 230. However, all cell bus data lines 550, cell bus clock signal lines 530 and cell bus sync lines 540 form a single (shared) bus between the AFIU 240 and the OLUs 230:

> As shown in FIG. 5, a cell bus 500 couples a plurality of optical line units (OLUs) 230 with the CRU 220 and the AFIU 240. For this embodiment, the cell bus 500 includes: cell clock lines 530, cell sync lines 540, and data lines 550.

Dove, column 7, lines 15–19. Contrary to the assertion within the final rejection, *Dove* depicts only a single cell bus, not multiple serial links for each interface control processor slot as recited in the claims.

2. The rejection of claims 1–4, 7–8 and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al.*

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 3 August 2005). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

Independent claims 1 and 20 each recite that the low tier comprises a cell-based bus capable of lower aggregate traffic rates (up to approximately two gigabits per second), while the high tier

comprises one or more serial links capable of higher aggregate traffic rates (up to approximately twenty gigabits per second). Such a feature is not found in the cited references.

Manchester et al, cited in the final rejection as satisfying these limitations, teaches a low-speed TDM bus 70 comprising point-to-point serial links and a high-speed ATM (cell-based) bus 72. *Manchester et al*, column 8, lines 19–47. *Manchester et al* specifically states that the traffic rates on TDM bus 70 are slower than those on ATM bus 72. *Manchester et al*, column 8, lines 21–23. The structure disclosed in *Manchester et al* is thus precisely the opposite of the structure that is recited in the claims: the cell-based bus 72 in *Manchester et al* provides a high speed connection rather than a lower speed connection as required in the claims for the recited cell-based bus, while the serial bus 70 in *Manchester et al* provides a slower connection than bus 72 rather than the higher speed connection as required for the serial links recited in the claims.

Tabu et al discloses a network of small, medium and large cell switches 3100, 2100 and 1100 supporting switching rates of 156 Mbps, 2 Gbps and 20 Gbps, respectively. *Tabu et al* contains no teaching or suggestion of any of the switches 1100, 2100 and 3100 including both a cell bus and a serial link, or of a serial link supporting a 2 Gbps data rate in addition to switches 1100, 2100 and 3100. Neither *Manchester et al* nor *Tabu et al* provide any motivation or incentive for modifying the teachings of *Manchester et al* to implement a lower speed cell bus and a higher speed serial link, rather than vice versa.

3. The rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Chui et al.*

Claim 5 depends from independent claim 1, and therefore include the limitation(s) identified above in the discussion relating to claim 1. As noted above, claim 1 recites features not found in *Manchester et al* and *Tabu et al*, taken alone or in combination. Such features are also not found in the cited portions of *Chiu et al.*

Claim 5 recites that ATM cells are wrapped with a header to allow circuit board switching based on a connection map. Such a feature is not found in the cited references. The cited portion of *Chiu et al* does not, as asserted in the final rejection, teach that the header depicted in Figure 9 therein is used for circuit board level switching of ATM cells, but instead teaches precisely the opposite:

> The ECP processes cells received from the QE via the ECIC 1402 and forwards the cells to one of four CBMs 1408, a CBS, or an MCE 1404. Processing includes Cell Bus Header look-up from the Cell Bus Header RAM 1412 for cell bus traffic and Mulficast (MC) Address RAM 1414 lookup for multicast traffic. *For ATM traffic, the ECP simply forwards the cell to the CBS, without the Cell Bus Header look-up.*

Chiu et al, column 8, lines 38–45 (emphasis added). In addition, nothing in *Chiu et al* attributes the "fair rate-based cell traffic arbitration," "flexibility" or "performance improvement in the translation of cell routing information" specifically to the presence of a header wrapped around the ATM cell as asserted in the final rejection, rather than to the handling mechanisms and protocols employed.

4. The rejection of claim 6 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Lentz et al.*

Claim 6 depends from independent claim 1, and therefore include the limitation(s) identified above in the discussion relating to claim 1. As noted above, claim 1 recites features not found in *Manchester et al* and *Tabu et al*, taken alone or in combination. Such features are also not found in the cited portions of *Lentz et al.*

Claim 6 recites two parallel buses each having a 32-bit data path. Such a feature is not found in the cited reference. The final rejection relies on the mere existence of prior 32 bit data paths, providing no specific motivation or incentive to employing (two) 32 bit data paths in the low tier as recited in the claims.

5. The rejection of claim 9 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Pajowski et al.*

Claim 9 depends from independent claim 1, and therefore include the limitation(s) identified above in the discussion relating to claim 1. As noted above, claim 1 recites features not found in *Manchester et al* and *Tabu et al*, taken alone or in combination. Such features are also not found in the cited portions of *Pajowski et al.*

Claim 9 recites providing a redundant clock reference for the low tier. Such a feature is not found in the cited references. Nothing in either over *Manchester et al* or *Tabu et al* suggests that timing errors in (asynchronous) ATM buses of the type disclosed therein are such a problem as to

motivate one skilled in the art to look to clock redundancy for synchronous systems as disclosed in *Pajowski et al.*

6. The rejection of claims 14–16 under 35 U.S.C. § 103(a) as being unpatentable over *Dove*.

Claims 14–16 depend from independent claim 10, and therefore include the limitation(s) identified above in the discussion relating to claim 10. As noted above, claim 10 recites features not found in *Dove*. Nor has any motivation or incentive for modifying the structure disclosed in *Dove* to include such features been identified.

Claim 14 recites that the serial links operate at the same clock rate as the back plane. Such a feature is not found in the cited references. The portions of *Dove* cited in the final rejection state that the cell bus (NOT the serial links) is clocked at 100 MHz, but are silent as to the clocking rate of either the serial links or the backplane.

Claim 15 recites that the high speed serial link clock rate is 65.536 MHz. Claim 16 recites that the high speed serial link serialization/deserialization devices multiply the link clock rate by a factor of 20 and 8B/10B encode. The final rejection asserts that such features "would have been routine experimentation and optimization." However, such reasoning fails to establish a *prima facie* case of obviousness.

7. The rejection of claims 18–19 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Panzarella et al.*

Claims 18–19 depend from independent claim 1, and therefore include the limitation(s) identified above in the discussion relating to claim 1. As noted above, claim 1 recites features not found in *Manchester et al* and *Tabu et al*, taken alone or in combination. Such features are also not found in the cited portions of *Panzalrella et al.*

Claim 18 recites providing a time division multiplex bus, a communications bus, a common control bus and/or a Joint Test Access Group bus on the backplane. Such a feature is not found in the cited references. *Panzarella et al* merely discloses a backplane containing multiple buses, and does not suggest the specific buses recited in the claims or incorporating such buses for a particular purpose.

CONCLUSION

The cited references, taken alone or in combination, fail to disclose every limitation of the claimed invention. Therefore, the rejections of claims 10–13 and 17 under 35 U.S.C. § 102(e) and of claims 1–9, 14–16 and 18–19 under 35 U.S.C. § 103 are improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–20 in this application.

Respectfully submitted,

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Date: 1-8-2007

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CLAIMS APPENDIX

1. For use in association with devices such as processors and modems used in wireless and wireline access systems, a backplane comprising:

a low tier that comprises a cell-based bus capable of aggregate traffic rates of up to approximately two gigabits per second; and

a high tier that comprises one or more serial links capable of aggregate traffic rates of up to approximately twenty gigabits per second.

2. The backplane as set forth in Claim 1 wherein said low tier that is capable of aggregate traffic rates of up to approximately two gigabits per second comprises:

a low tier bus comprising a switching architecture that (1) allows a circuit board card on an input side of a connection to transmit data to a circuit board card on an output side of said connection, and that (2) allows a circuit board card on the output side of a connection to receive data from a circuit board on the input side of said connection.

3. The backplane as set forth in Claim 2 wherein said low tier bus supports one of: packet based traffic, unicast traffic, multicast traffic, and broadcast traffic.

4. The backplane as set forth in Claim 2 wherein said low tier bus supports asynchronous transfer mode traffic.

5. The backplane as set forth in Claim 4 wherein said low tier bus wraps asynchronous transfer mode cells with a header to allow said low tier bus to switch cell based traffic according to a connection map on each circuit board card connected to said low tier bus.

6. The backplane as set forth in Claim 2 wherein said low tier bus comprises two (2) parallel busses, each of which comprises a thirty two (32) bit data path.

7. The backplane as set forth in Claim 2 wherein said low tier bus operates at a clock rate equal to one half of a clock rate of said backplane.

8. The backplane as set forth in Claim 7 wherein said low tier bus clock rate is 32.768 MHz.

9. The backplane as set forth in Claim 2 comprising a redundant clock reference for said low tier bus.

10. For use in association with devices such as processors and modems used in wireless and wireline access systems, a backplane comprising:

a high tier that comprises one or more serial links capable of aggregate traffic rates of up to approximately twenty gigabits per second.

11. The backplane as set forth in Claim 10 wherein said high tier that is capable of aggregate traffic rates of up to approximately twenty gigabits per second comprises:

a high tier bus; and

at least two switch matrix circuit board cards coupled to said high tier bus.

12. The backplane as set forth in Claim 11 wherein said high tier bus comprises:

high speed serial links coupled to said at least two switch matrix circuit board cards and coupled to any other circuit board cards capable of sending and receiving high speed data traffic.

13. The backplane as set forth in Claim 12 wherein said high speed serial links comprise:

point-to-point serial links comprising differential pairs for both a transmit path and a receive path.

14. The backplane as set forth in Claim 13 wherein said high speed serial links operate at a clock rate equal to a clock rate of said backplane.

15. The backplane as set forth in Claim 14 wherein said high speed serial link clock rate is 65.536 MHz.

16. The backplane as set forth in Claim 14 comprising a high speed serial link serial/de-serial device that multiplies said high speed serial link clock rate by a factor of twenty (20), and wherein each high speed serial link is 8B/10B encoded.

17. The backplane as set forth in Claim 12 comprising at least two (2) high speed serial links for each interface control processor slot in said backplane.

18. The backplane as set forth in Claim 1 further comprising one of: a time division multiplex bus, a communications bus, a common control bus, and a Joint Test Access Group test bus.

19. The backplane as set forth in Claim 18 further comprising at least one set of clock and framing resources.

20. A device comprising a backplane comprising:

a low tier that comprises a cell-based bus capable of aggregate traffic rates of up to approximately two gigabits per second; and

a high tier that comprises one or more serial links capable of aggregate traffic rates of up to approximately twenty gigabits per second;

wherein said device comprises one of: an access processor unit, a modem unit, and a combined access processor and modem unit.

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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.